

Qimonda Develops High-Speed Data Interface for First-Silicon-Right Chip Based on GDDR5 in Record Time

High-performance graphic applications for game consoles, desktop PCs, and notebooks have an insatiable appetite for faster dynamic random access memory (DRAM). The new graphic memory standard, Graphics Double Data Rate version 5 (GDDR5), is the next step in meeting this demand, providing a 300% performance increase over today's GDDR3 chips.

Engineers at Qimonda design GDDR5-compliant semiconductors using MathWorks™ tools and Model-Based Design, an approach that enables them to verify performance before committing to silicon.

“Using MATLAB® and Simulink®, we can combine functional and analytical descriptions of our design, which is a tremendous advantage,” explains Dr. Peter Gregorius, Principal Engineer at Qimonda. “It means that we can verify our design under a range of operating conditions without having to create a test chip.”

THE CHALLENGE

A key technical challenge for Qimonda was to optimize the DRAM chip's internal clock and data paths for communication between the memory and memory controller. “The high data rates required by GDDR5 are close to the limit of what is physically possible,” says Gregorius. “At these rates, a clock or data path that bridges distances over several millimetres can suffer from signal integrity issues.”

To optimize the chip's internal clock and data buses, Qimonda needed to combine a functional model of the memory with a model based on the connection between the memory



Qimonda's GDDR5-compliant DRAM chip.

and memory controller—including channel characteristics, delay and noise formulas for capacitive, and inductive coupled metal lines.

The design needed to achieve low bit error rates and high data rates under conditions including disturbances in voltage, variations in temperature, and mechanical stress.

Short product cycles and market demand for low-cost, low-power devices imposed additional constraints.

As part of the standardization effort, Qimonda needed to share aspects of their design with the GDDR5 standards consortium and with business partners who were developing memory controllers for the Qimonda GDDR5 DRAM.

THE SOLUTION

Qimonda used MathWorks tools for Model-Based Design to model the functional and physical characteristics of the GDDR5 memory design, optimize the chip floor plan, and verify performance.

Using Simulink, Communications Blockset™, and Signal Processing Blockset™, engineers combined functions that typically

THE CHALLENGE

To reduce time-to-market for the next generation of high-performance graphics memory

THE SOLUTION

Use MathWorks™ tools and Model-Based Design to develop and verify chip design by combining functional and analytical models

THE RESULTS

- Time-to-market reduced by six months
- Detailed design specifications provided to business partners
- Design quickly adapted to meet evolving requirements

required multiple tools into a single, multi-domain system model of the GDDR5. The model incorporated sources and sinks from Communications Blockset, as well as delay-locked loops and phase-locked loops from Qimonda's library of custom Simulink blocks. Using Filter Design Toolbox™, the engineers modeled the step response of buffers and other transistor-level blocks.

A complete GDDR5 system requires a complex training sequence for the chip-to-chip interconnections between the memory controller and the memory. To find an optimal training sequence, Qimonda used a Simulink model consisting of a memory controller model, a channel model, and a detailed model of the memory.

With MATLAB, they initiated multiple Simulink simulations, sweeping variables such as power sensitivity, noise, temperature, delays, and mechanical stress, and developed sophisticated algorithms for post-processing the simulation results and calculating noise statistics for the nonlinear circuit.

Gregorius delivered an executable specification to the circuit design team that included simulation results, clock and data tree models, pre-dimensioned transistor-level building blocks, and a set of geometrical dimensions of interconnects that minimizes noise, delay, and power sensitivity. The circuit designers used this executable specification to accelerate transistor-level design.

Qimonda has shipped fully functional GDDR5 DRAM samples to business partners. Qimonda engineers are reusing their Simulink models as they develop the next version of the device.

APPLICATION AREAS

- Data analysis
- Electronics
- Semiconductors
- Signal processing

PRODUCTS USED

- MATLAB®
- Simulink®
- Communications Blockset™
- Signal Processing Blockset™
- Filter Design Toolbox™

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Using MATLAB® and Simulink® we developed a complex design that combined functional and analytical models of our device. Model-Based Design enabled us to perform faster iterations to optimize performance, quality, and power efficiency – before going to silicon. By getting the information we needed from our model, we eliminated the delay and expense of making a test chip.

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Dr. Peter Gregorius, Qimonda

THE RESULTS

▪ **Time-to-market reduced by six months.** “Using MathWorks tools for system design and verification enabled us to complete our GDDR5 memory in one design cycle,” says Gregorius. “By getting first-silicon-right, we eliminated a redesign cycle of about six months.”

▪ **Detailed design specifications provided to business partners.** “We shared our MATLAB and Simulink models with our business partners and the GDDR5 standards consortium,” notes Gregorius. “Our partners used them to optimize the design of memory controllers before our chip was ready. This gives us an advantage over our competitors because we can provide our partners with detailed information on how to use our device to ensure maximum reliability.”

▪ **Design quickly adapted to meet evolving requirements.** “Simulink provided us with the flexibility to adapt our design as the GDDR5 standard evolved,” says Gregorius. “At one point we had to double one of our internal clock rates. With MathWorks tools and Model-Based Design, we made and verified the changes in about a week.”

To learn more about Qimonda, visit www.qimonda.com

