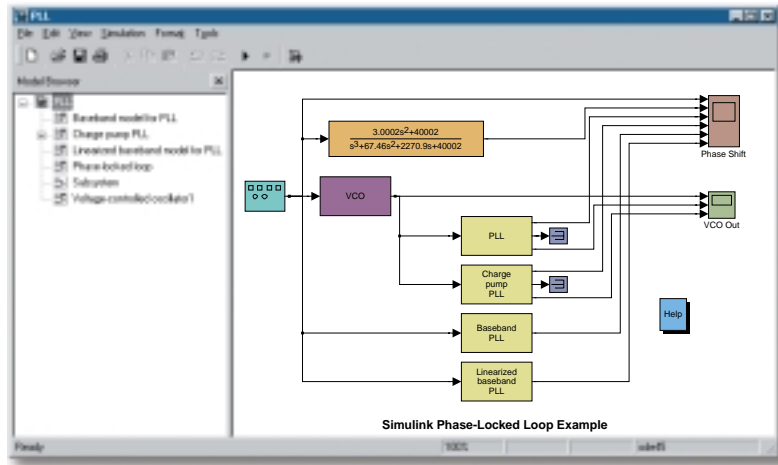


Motorola Accelerates Simulation with Simulink®



Simulink's intuitive block-diagram environment helped Motorola develop fast, accurate predictions of phase-locked loop performance.

THE CHALLENGE

To achieve fast, accurate simulations of phase-lock loops

THE SOLUTION

Simulate phase-lock loops using MathWorks system-level design and simulation products for high performance, high analog and digital resolution, and mixed-signal systems.

THE RESULTS

- Accelerated simulations
- Seamless C coding
- Transferable technology

New production specifications for the Wireless Subscriber Systems Group at Motorola required engineers to search for tools that would dramatically reduce simulation speed. Using Simulink® in conjunction with MATLAB® and Real-Time Workshop®, they succeeded in reducing simulation time for a 100-microsecond test from two hours to just 1.2 minutes, far less than the time specified.

THE CHALLENGE

At the design center of Motorola's Wireless Subscriber Systems Group (WSSG), engineers working on mixed-signal phase-lock loop (PLL) simulations faced obstacles to achieving faster design cycles, including long runtimes and poor simulation resolution.

Motorola's WSSG engineers employ PLLs for carrier tracking, threshold extension, linear demodulation, amplitude detection, and synchronization. As PLLs get used in mixed-signal integrated circuits and move to higher frequencies, the need for quick, accurate simulations has become a priority. Motorola's transistor-level mixed-mode SPICE/Verilog models took nearly two days to run. The new Motorola

specifications called for reducing simulation time to less than two hours for a 600-microsecond simulation. To meet the new requirements, the models also had to have a 1-pico-second resolution, allow for the simulation of noisy signals, work on multiple platforms, be easy to use, and offer an open environment.

A PLL must be modeled as a combination of digital and analog subsystems to accurately predict phenomena such as cycle-to-cycle jitter and sensitivity of the loop locking to noise. A successful simulator needs to be able to handle mixed analog and digital signals with accurate representation of the noise signals and still perform efficiently over a large number of clock cycles.

"We were looking for tools that would help us meet our project specifications and could be transferred to other groups within Motorola," said Jeff Ganger, principle staff engineer with the Wireless Integration Technology Center, who was in charge of the PLL project.

Ganger's group first tried a higher-level version of their mixed-mode SPICE/Verilog simulator, replacing the digital portions with Verilog behavioral models while keeping the

analog portion modeled at the transistor level with SPICE. The result was a simulation that took nearly two hours for a 100-microsecond test. Engineers estimated that a 600-microsecond simulation would take ten hours, well beyond the specification.

THE SOLUTION

Ganger's group found their solution with the high-performance, Simulink behavioral simulation environment. Simulink is ideal for mixed-signal simulations because it lets engineers achieve quality analog resolution with true continuous-time solvers and zero crossing methods without sacrificing simulation speed. Initial tests showed that a Simulink model could run a 100-microsecond simulation with sub-picosecond resolution in just ten minutes, immediately eliminating the SPICE model from consideration.

In addition to simulation speed, engineers were able to take advantage of other capabilities that only Simulink could offer: support for analog mixed-signal systems, an extensive library of prepackaged blocks, and state-of-the-art zero crossing methods that let engineers maintain overall simulation speed while precisely detecting discontinuities in a signal.

While simulation speed was their primary concern, the WSSG's decision to invest in Simulink was also influenced by other factors, including its availability for both PC and UNIX systems, ease of use, support for mixed-signal simulations, and handling of multirate system sampling.

Having met project requirements with the pure Simulink model, WSSG engineers then took advantage of Simulink's mixed-signal capabilities and investigated the tradeoffs between simulation speed and resolution. They improved results even further by

“The Simulink models exceeded our project specifications for required simulation speed. Accurate simulations can now be measured in minutes rather than hours or days.”

Yuan Yuan, Motorola

replacing some analog component models with discrete approximations and by using Real-Time Workshop to automatically generate C code from the Simulink model.

Summing up the experience, Jeff Ganger said “Our reservations about using a behavioral modeling tool like Simulink disappeared once the tests were completed. Simulink has proven itself with our team as an industrial-strength design and simulation environment.”

THE RESULTS

- **Accelerated simulations.** The modified simulation ran at an impressive 2.5 minutes per 100-microsecond simulation, significantly faster than specification requirements.
- **Seamless C coding.** The team took advantage of the seamless C interface in Simulink. They recoded computationally intensive components of the models in C and reduced the simulation time still further, to just 1.2 minutes.
- **Transferable technology.** Having used Simulink to meet the WSSG's demands, the proven Simulink technology could then be used by other PC- and UNIX-based systems at Motorola

To find out more about the Wireless Subscriber Division of Motorola, visit www.motorola.com/wireless-semi

APPLICATION AREAS

- Electronics
- Wireless communications
- Modeling and simulation

PRODUCTS USED

- MATLAB®
- Simulink®
- Real-Time Workshop®

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