

Sandia Implements a High-Performance Radar Receiver Using MathWorks and Xilinx DSP Design Tools

Field programmable gate arrays (FPGAs) have wider potential than application-specific integrated circuits (ASICs) because they can be programmed in the field even after customer installation, allowing for future upgrades and enhancements. Implementing designs on an FPGA, however, requires tight integration among several teams. Typically, DSP designers are unfamiliar with FPGA design tools, and FPGA designers are unfamiliar with DSP algorithms.

Sandia National Laboratories have increased efficiency by designing and simulating DSP systems with MATLAB® and Simulink®. They then use Xilinx Virtex-II FPGAs and DSP modeling and implementation tools to test and verify the hardware.

"Having MATLAB and Simulink so tightly integrated with the Xilinx toolset is a real asset for Sandia," says Dale Dubbert, digital radar development project lead at Sandia. "We are so impressed with the tools and the direction in which The MathWorks and Xilinx are going that we plan to make this our mainstream DSP design flow."

This environment is enabling Sandia to save time in developing a digital IF receiver for a high-performance Synthetic Aperture Radar (SAR) system.

THE CHALLENGE

Electronics system designers at Sandia's Synthetic Aperture Radar Department are replacing a SAR analog IF receiver module set with a digital implementation. The current SAR system is housed in a VME (Versa Module Europa) chassis, where the digital receiver and related hardware, using Xilinx Virtex-II FPGAs, will also reside.



The first prototype of the digital IF receiver module.

SAR systems are ideal for surveillance projects that require imaging of a broad area at high resolution, during difficult weather conditions, or at night. For example, they provide terrain structural information to geologists for mineral exploration and sea state and ice hazard maps to navigators. Their complexity, however, makes them challenging to design.

Sandia's SAR digital processors will process high rates of data and must meet other stringent performance and output requirements. In addition, the digital IF receiver module is to be run at a higher level of FPGA integration than Sandia has ever attempted before in a radar system.

The software for implementing the DSP subsystem needs to be inexpensive and relatively easy to use. It is also important for the DSP and FPGA designers to work closely together.

THE SOLUTION

Sandia uses MathWorks and Xilinx DSP design tools, including MATLAB, Simulink, the Xilinx System Generator for DSP (System Generator), and Xilinx ISE FPGA implementation tools, to program and verify the FPGA.

THE CHALLENGE

To design a digital radar receiver and implement it on the Virtex-II platform FPGA within strict time and budgetary limits

THE SOLUTION

Use MathWorks and Xilinx DSP design software to create, simulate, test, and synthesize designs into hardware.

THE RESULTS

- Accelerated design
- High-speed simulation
- Accurate representation of the actual system

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Dale Dubbert, Sandia National Laboratories

Sandia engineers designed, simulated, implemented, and tested each DSP building block individually in the Virtex-II platform FPGA. DSP engineers modeled several DSP functional blocks in Simulink. They then used the System Generator to generate VHDL code and map certain blocks to the preverified soft DSP cores provided in the Xilinx DSP core library.

An important component of the system is a highly parallel polyphase decimation FIR filter/demodulator. This fixed-point, multirate filter was easy to design using Simulink and the Filter Design Toolbox. Sandia designers could easily create the quantized filter coefficients in the Filter Design and Analysis Tool in the Signal Processing Toolbox and import them into the MATLAB workspace. From there, they created a block diagram design of the filter using the Fixed-Point Blockset.

Sandia used MATLAB to analyze the filter's performance by sending the outputs from the Simulink – System Generator model as a complex vector to the MATLAB workspace, where a MATLAB callback function calculated and displayed the filter/demodulator output spectrum. An interface was designed to provide easy access to key functions.

The MATLAB and Simulink environment was used to test the designs in hardware to reduce the risk of creating difficult-to-diagnose problems at integration time. Other components of the system were modeled in a similar way.

The DSP system is currently being implemented in hardware using Xilinx ISE implementation software and two XC2V6000 (six million gate) Virtex-II FPGAs.

THE RESULTS

- **Accelerated design.** Traditional DSP design methods would have taken multiple iterations. The System Generator saved time by allowing the DSP designer to create new designs or modify existing designs, simulate them in Simulink, and then synthesize them into hardware.
- **High-speed simulation.** The digital IF receiver module, using two XC2V6000 FPGAs, will run at an estimated 20 to 25 gigaMACs per second, orders of magnitude higher levels of FPGA integration than Sandia has ever attempted in a radar system.
- **Accurate representation of the actual system.** Once the entire system was modeled using Simulink, Sandia's engineers were confident that the model would be a bit-true representation of what would be implemented onto the FPGA.

To learn more about Sandia, visit

www.sandia.gov

APPLICATION AREAS

- Digital signal processing
- System-level design

PRODUCTS USED

- MATLAB*
- Simulink*
- Filter Design Toolbox
- Signal Processing Toolbox
- Fixed-Point Blockset
- Xilinx System Generator for DSP

www.mathworks.com