

Simulink® HDL Coder 1

Generate synthesizable HDL Code from Simulink models and Stateflow diagrams

Simulink® HDL Coder generates bit-true, cycle-accurate, synthesizable Verilog and VHDL code from Simulink® models and Stateflow® diagrams. The automatically generated HDL code is target independent.

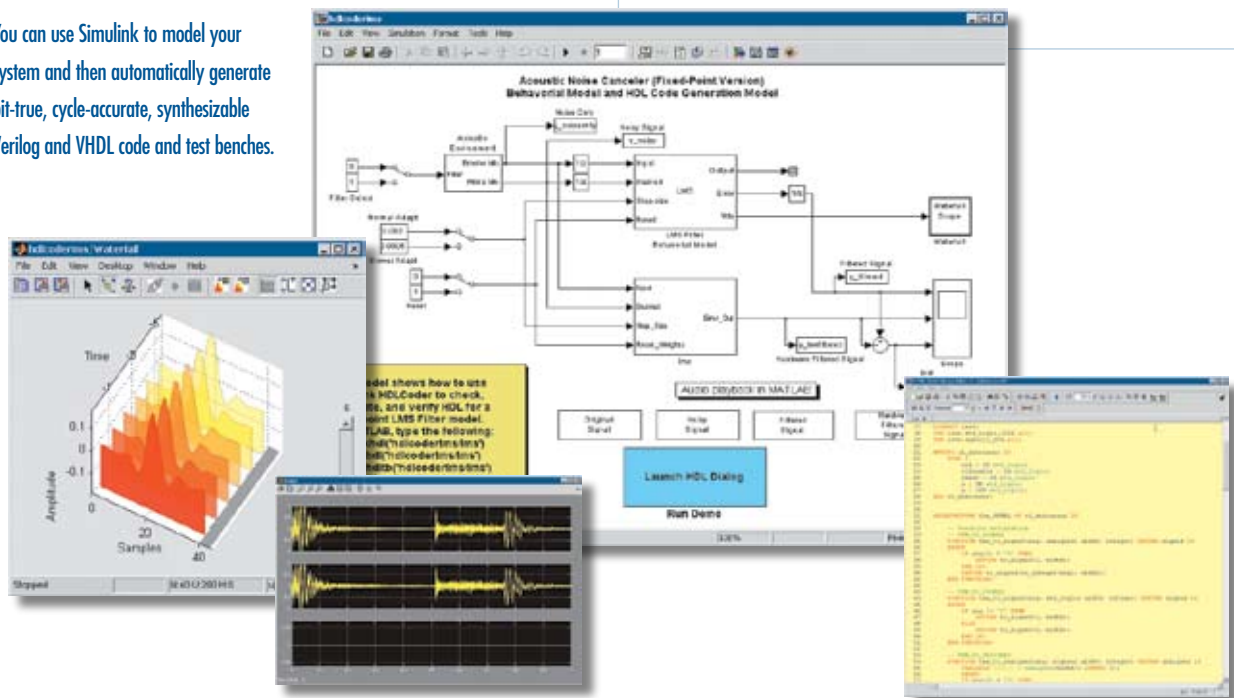
You can simulate and synthesize the automatically generated HDL code using industry-standard tools and then map it into field-programmable gate arrays (FPGAs) or application-specific integrated circuits (ASICs). You can also use the automatically generated HDL code to verify existing HDL code using formal or functional verification tools.

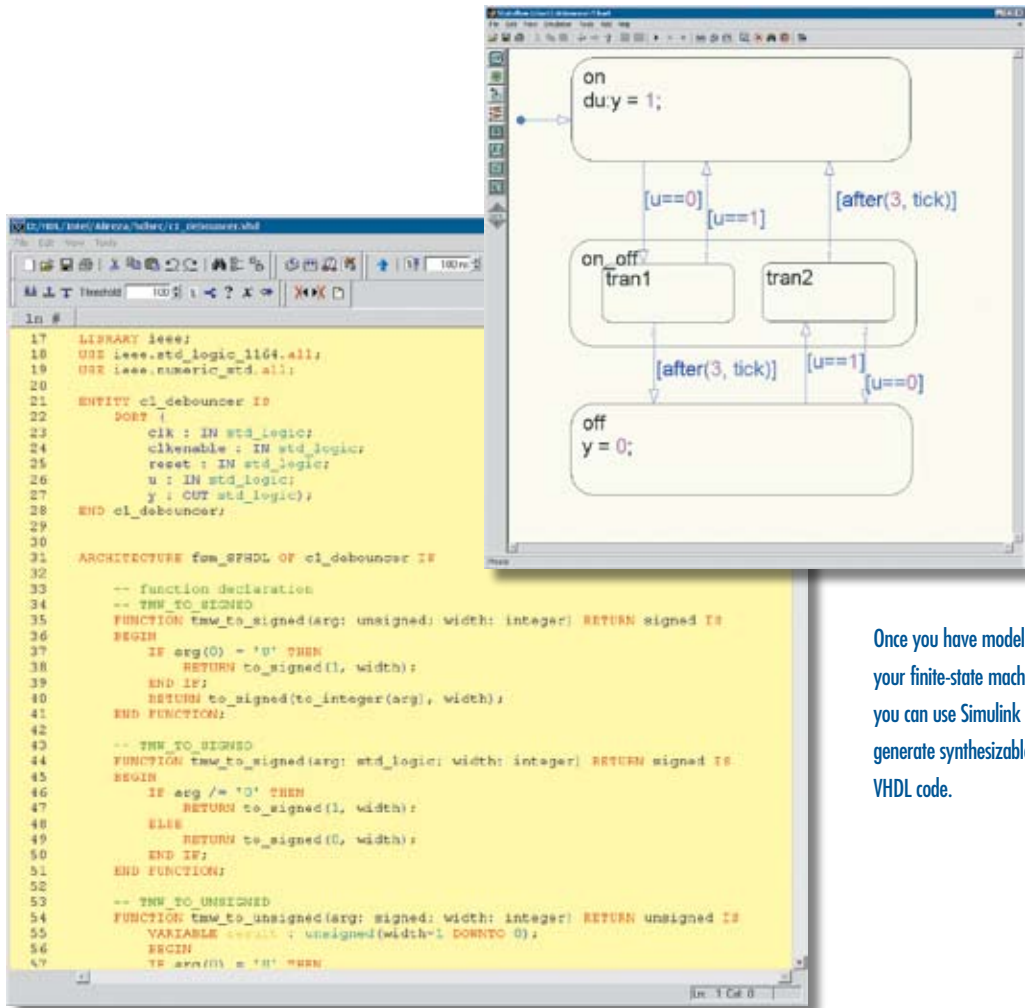
Simulink HDL Coder also generates test benches, enabling rapid verification of the generated HDL code using HDL simulation tools.

KEY FEATURES

- Generates synthesizable HDL code from Simulink models for datapath implementations
- Generates synthesizable HDL code from Stateflow diagrams for Mealy and Moore finite-state machines and control logic implementations
- Generates VHDL code that is IEEE 1076 compliant and Verilog code that is IEEE 1364-2001 compliant
- Lets you create bit-true and cycle-accurate models that match your Simulink design specifications
- Incorporates multirate Simulink models in one HDL clock domain
- Lets you select from multiple HDL architectural implementations for commonly used blocks
- Lets you specify the subsystem for HDL code generation
- Enables you to reuse existing IP HDL code (with Link for ModelSim®, available separately)
- Generates simulation and synthesis scripts

You can use Simulink to model your system and then automatically generate bit-true, cycle-accurate, synthesizable Verilog and VHDL code and test benches.





Once you have modeled and simulated your finite-state machines in Stateflow, you can use Simulink HDL Coder to generate synthesizable Verilog and VHDL code.

Working with Simulink HDL Coder

Simulink HDL Coder bridges the gap between system design and hardware implementation. It lets you generate synthesizable, correct-by-construction HDL code that can be used to rapidly design, verify, and develop prototypes of signal processing algorithms. By using Simulink HDL Coder, you can model your system in Simulink and Stateflow and then generate HDL code for the datapath and control sections of your design.

Simulink HDL Coder provides multiple options that let you control the type and structure of HDL code. You can use the built-in graphical user interface (GUI) or a code generation control file to make your selections. You can choose the polarity, type, and port name of the reset signal along with language-specific options for Verilog and VHDL. You can also define a default HDL code generation template that can be used across the organization.

You can use the automatically generated Verilog and VHDL code for rapid prototyping, formal and functional verification of hand-coded HDL, and other applications. Simulink HDL Coder generates simulation and synthesis scripts that enable you to quickly simulate and synthesize your design.

Using Simulink HDL Coder with Link for ModelSim

When you use Simulink HDL Coder with Link for ModelSim, you can incorporate existing HDL code and IP blocks, such as memories and hard macros, into your Simulink model. You simply instantiate a Link for ModelSim block in your Simulink model and define its I/O ports so that they correspond to the I/O ports of your IP. HDL code generated for the subsystem containing the Link for ModelSim block includes the port definition for your IP, enabling you to integrate your IP with automatically generated HDL.

Required Products

MATLAB®

Simulink

Fixed-Point Toolbox

Simulink® Fixed Point

Related Products

Filter Design HDL Coder. Generate VHDL and Verilog code for fixed-point filters from MATLAB

Link for ModelSim. Cosimulate and verify VHDL and Verilog using ModelSim®

Signal Processing Blockset. Design and simulate signal processing systems and devices

Signal Processing Toolbox. Perform signal processing, analysis, and algorithm development

Stateflow. Design and simulate state machines and control logic

Platform and System Requirements

For platform and system requirements, visit www.mathworks.com/products/slhdlcoder

```
type('dct8control.m')

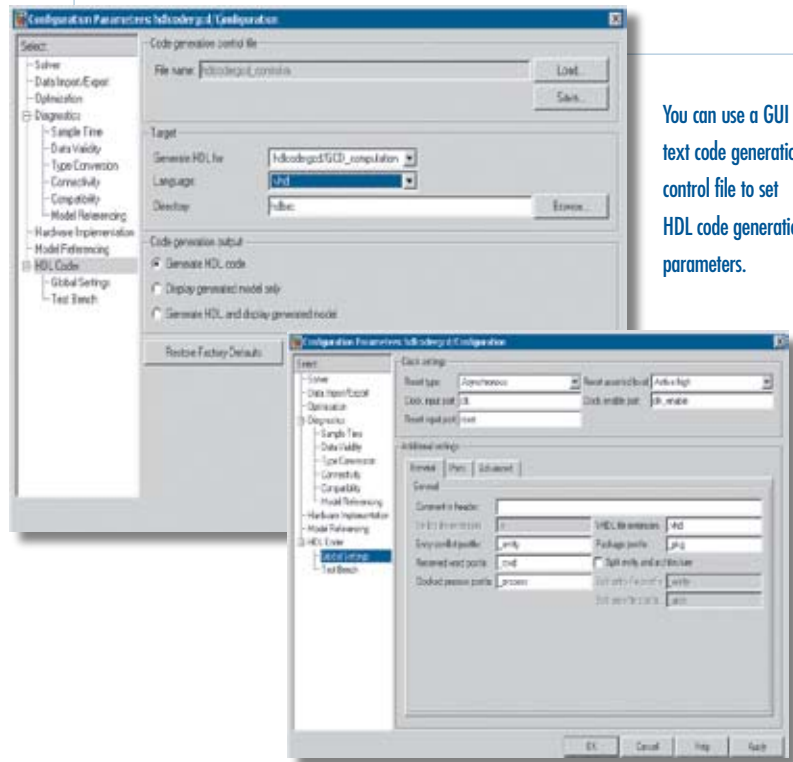
function c = dct8control
% C = DCT8CONTROL
% This is a sample control file for the Simulink HDL Coder
% dct8_fixed demo. This file shows how you can change the target
% language to Verilog and set the top-level using control
% files.

% Copyright 2006 The MathWorks, Inc.
% $Revision: 1.1.4.1 $ $Date: 2006/03/21 05:12:39 $

c = hdlnewcontrol(mfilename);

% First set for Verilog
c.set('TargetLang', 'Verilog');

% Now set the chip top-level
c.generateHDLFor('dct8_fixed/OneD_DCT8');
```



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